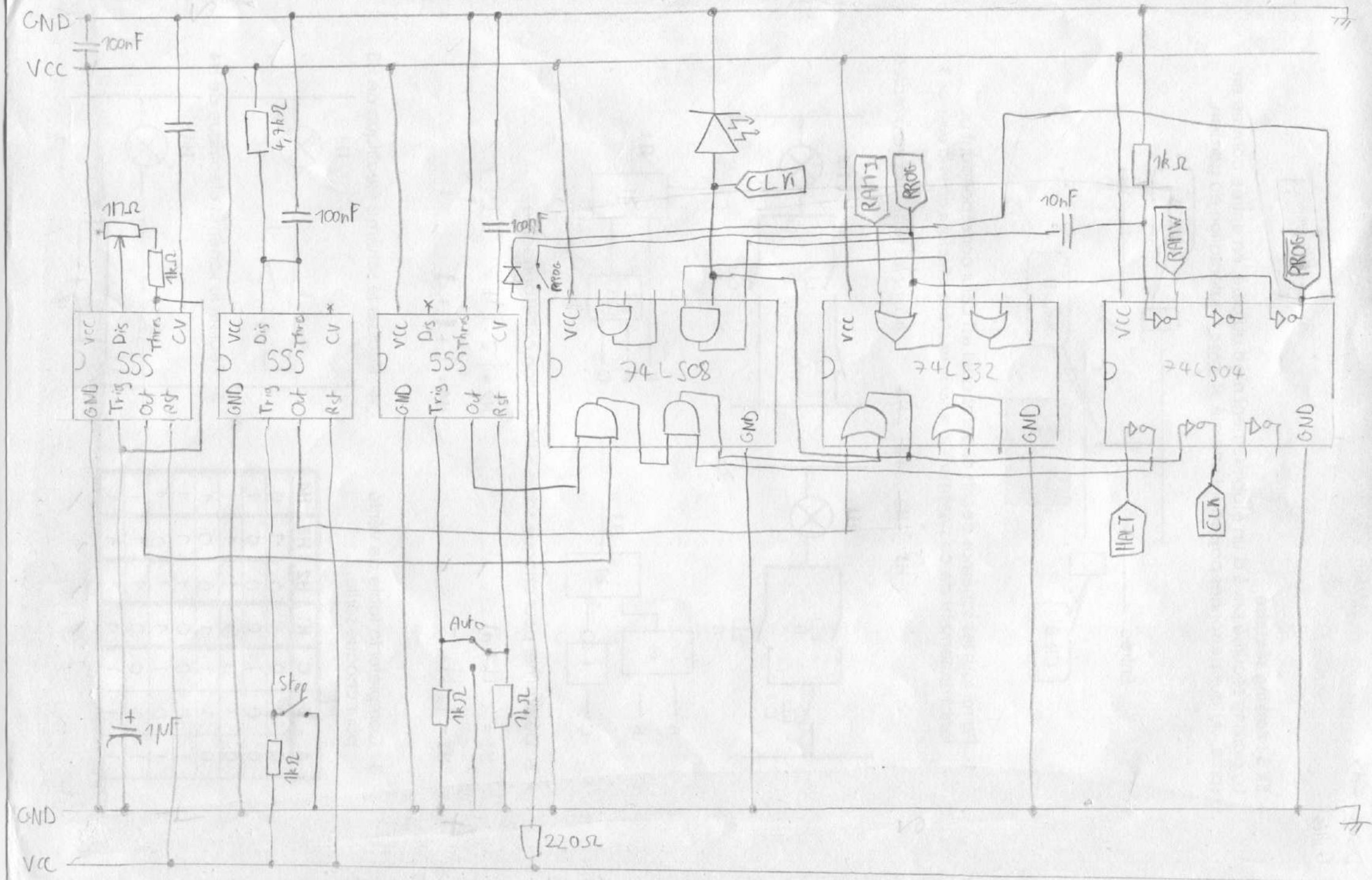
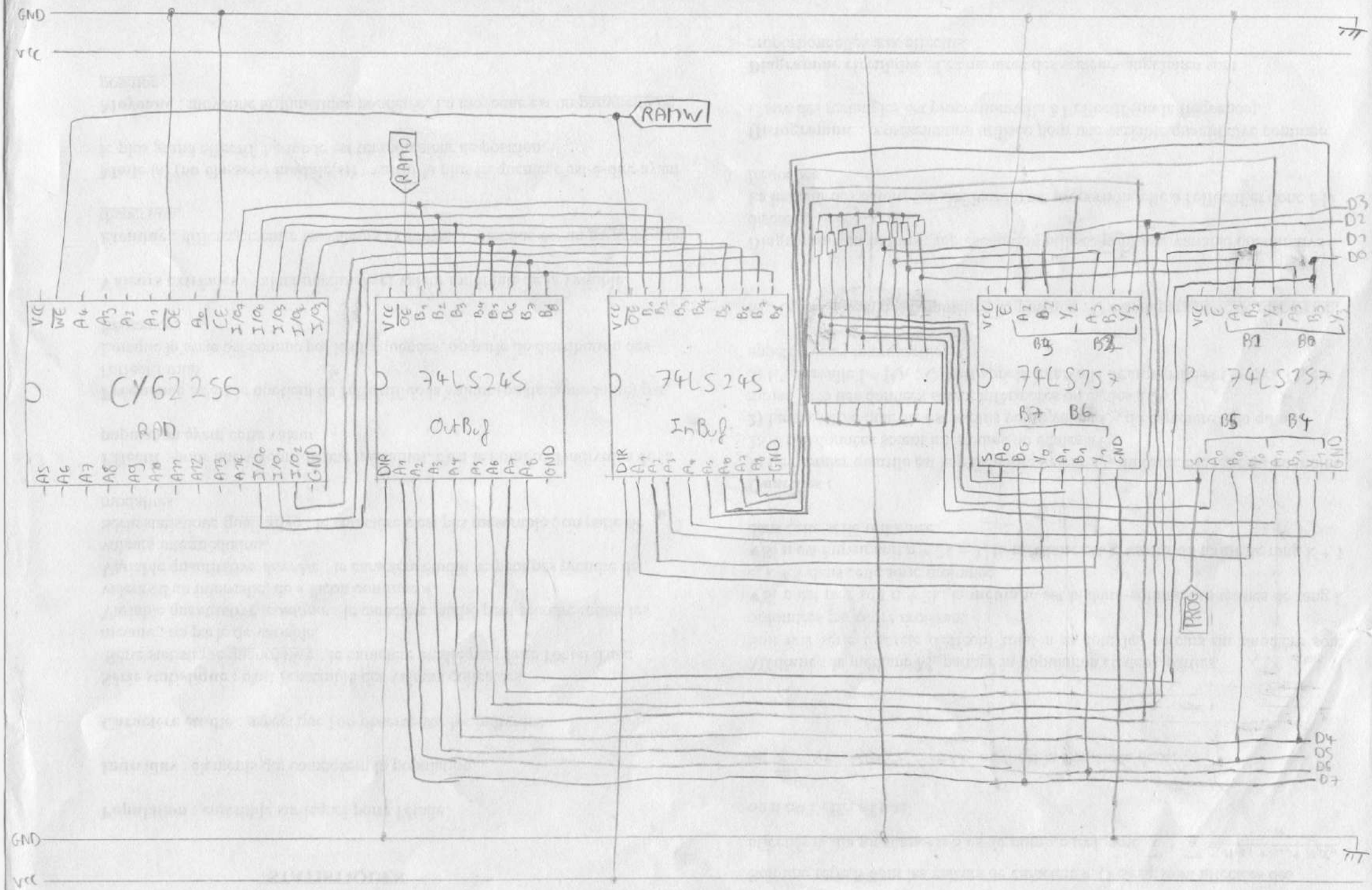
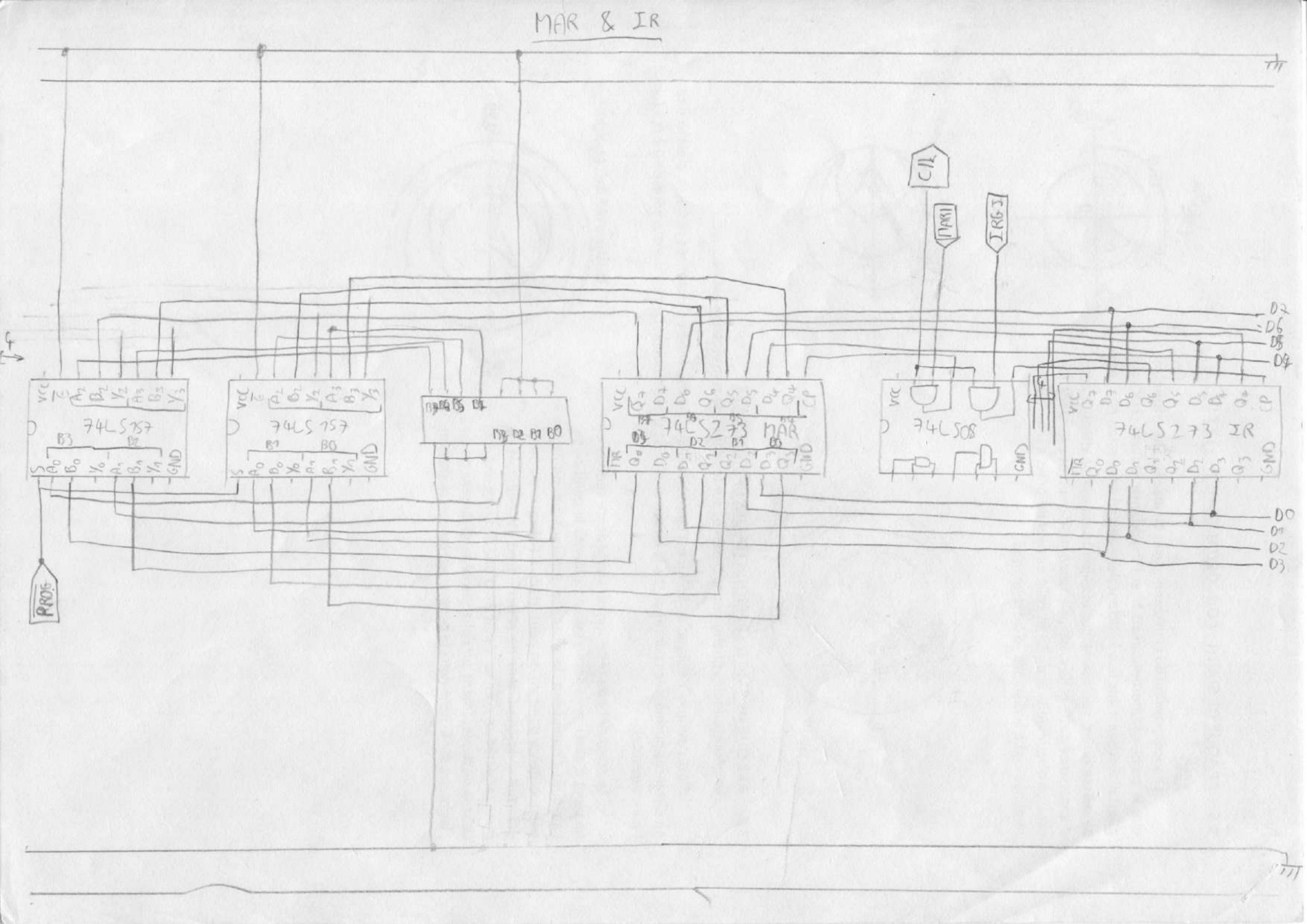
Clock


GND
VCC
100nF
4,7kΩ
100nF
1kΩ
100nF
CLK
RAM1
PROG
10nF
1kΩ
RAMW
PROG
555
555
555
74LS08
74LS32
74LS04
GND
HALT
CLK
Auto
Stop
1kΩ
1kΩ
1kΩ
1µF
220Ω
GND
VCC

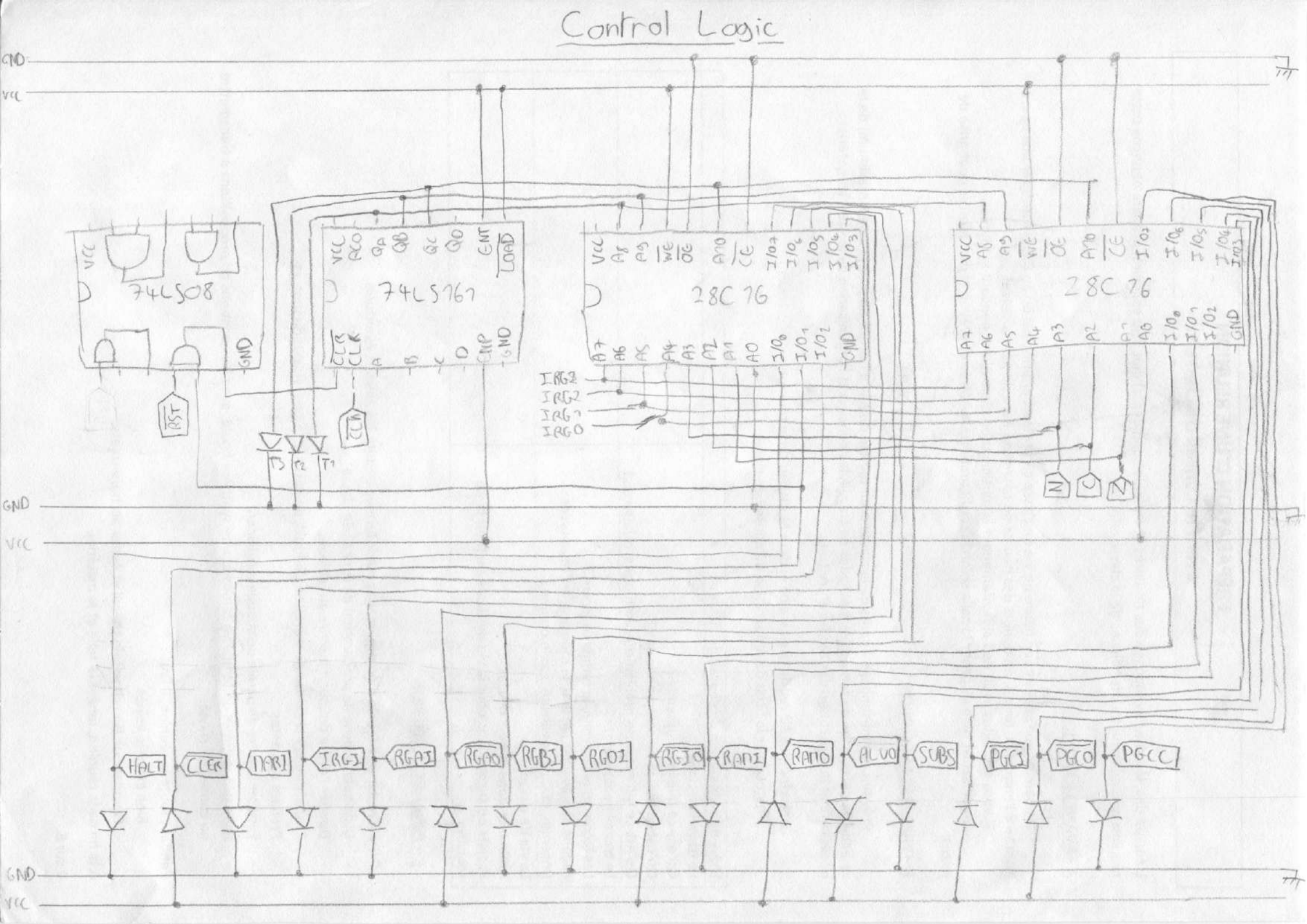
RAM


GND
VCC
RAMWI
RAMO
CY62256
RAM
74LS245
OutBuf
74LS245
InBuf
74LS757
74LS757
PROG
D3
D2
D1
D0
D4
D5
D6
D7
GND
VCC

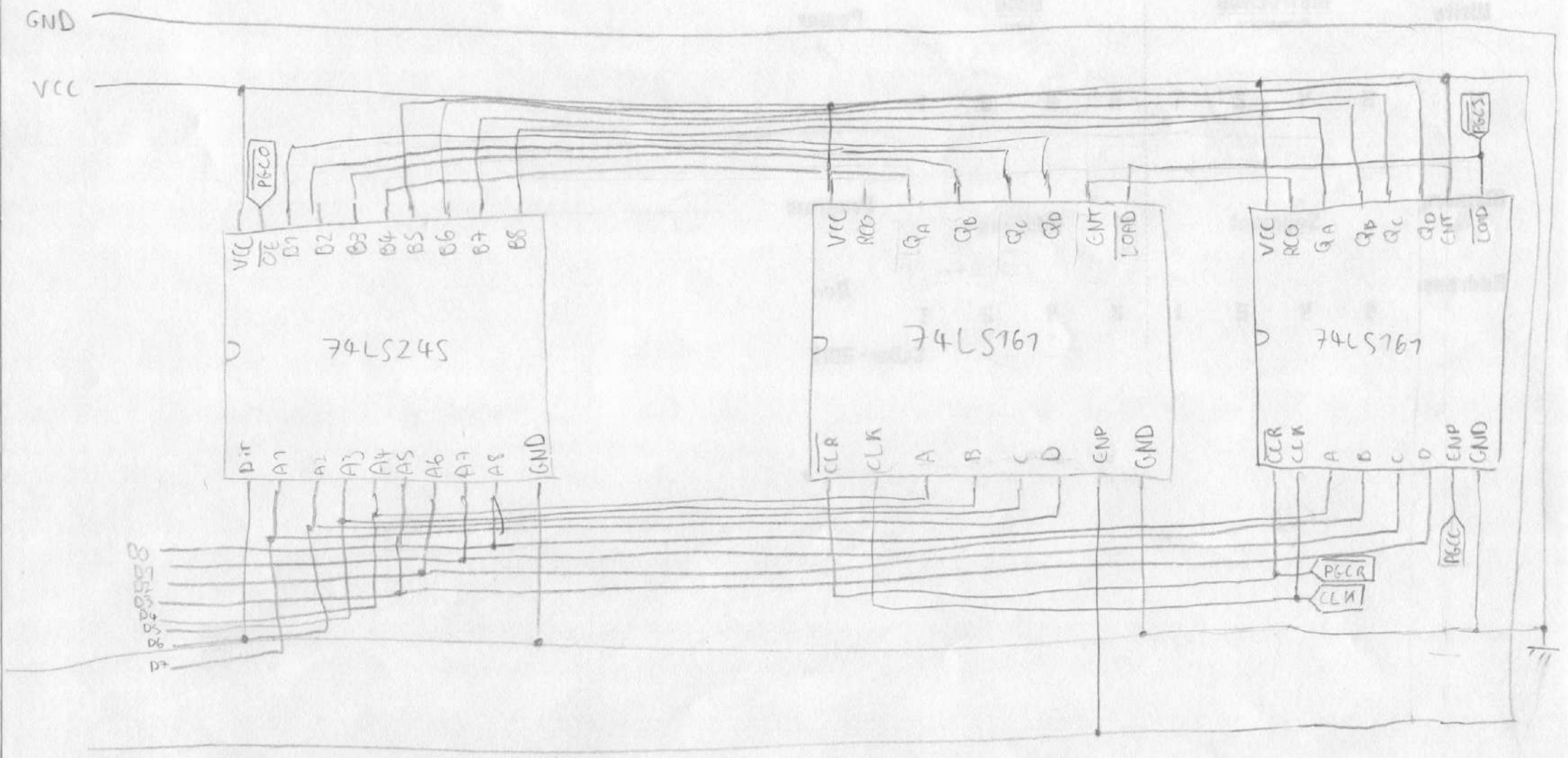
MAR & IR

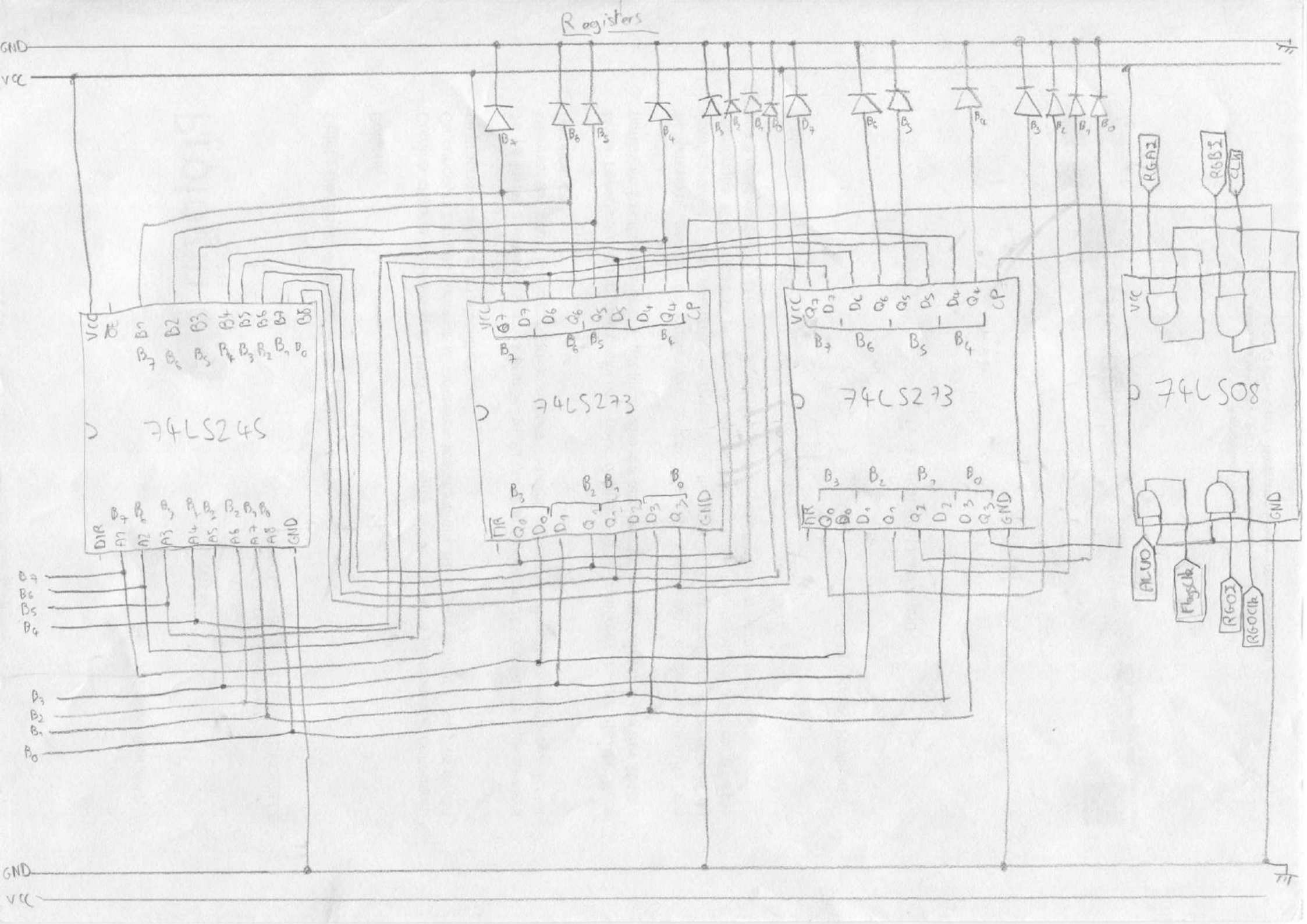

74LS157
74LS157
74LS273 MAR
74LS08
74LS273 IR
CIL
MAR1
IRG3
PROG
D2
D6
D5
D4
D0
D1
D2
D3

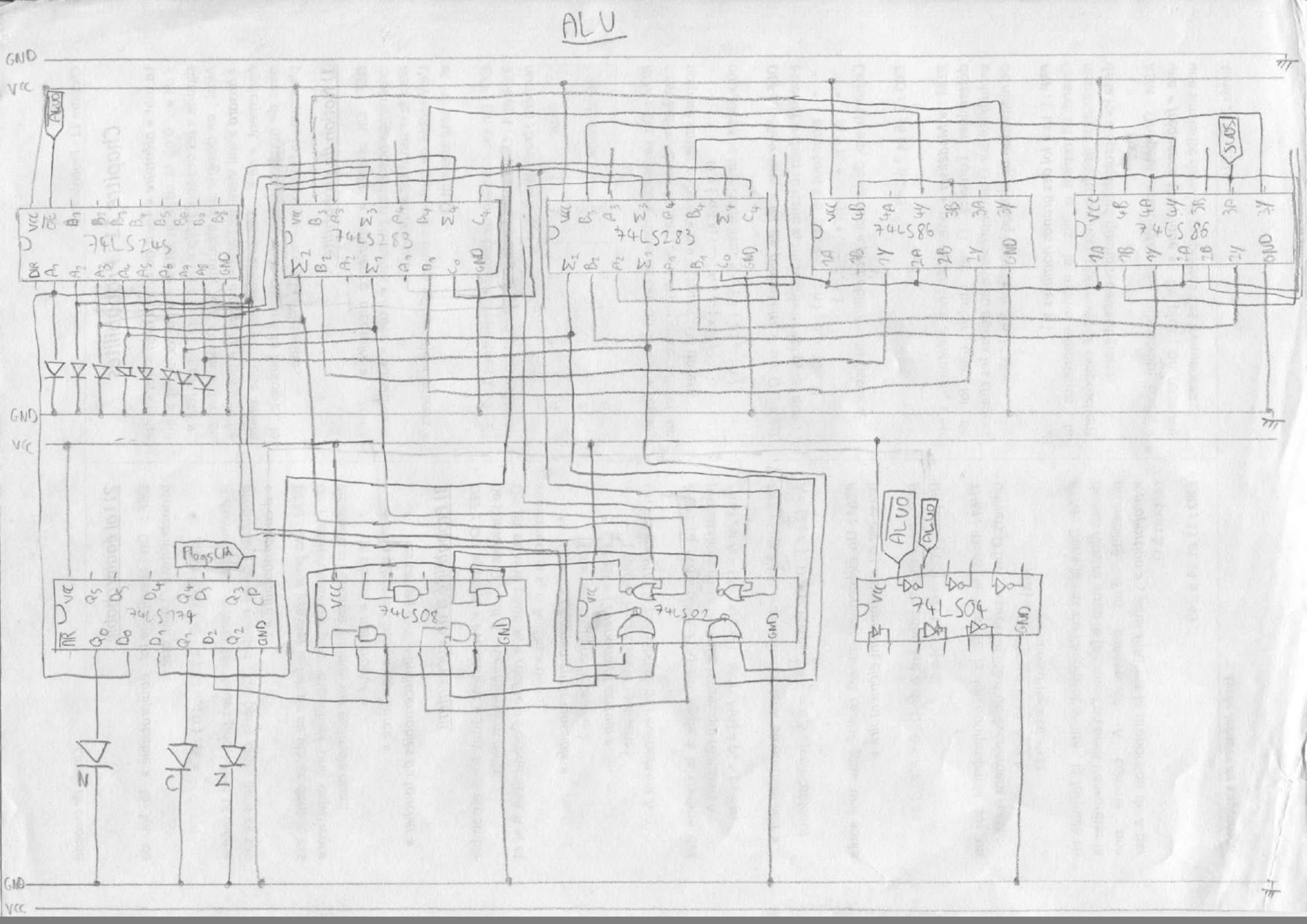
Control Logic



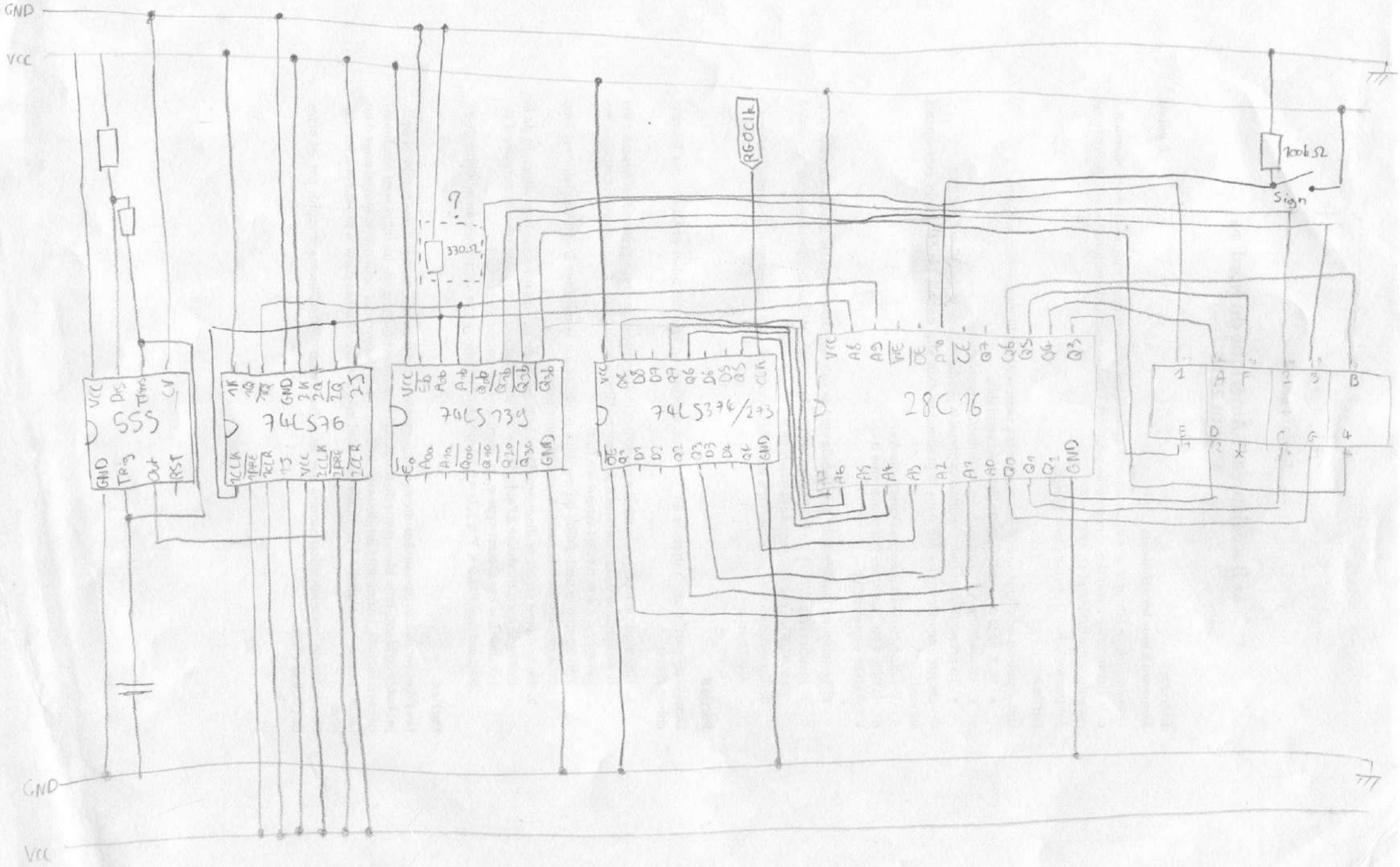
PC


GND
VCC
PGCO
74LS245
VCC
OE
D1
D2
D3
D4
D5
D6
D7
D8
DIR
A1
A2
A3
A4
A5
A6
A7
A8
GND
74LS161
VCC
RCO
QA
QB
QC
QD
CNT
LOAD
CLR
CLK
A
B
C
D
ENP
GND
PGCS
PGCR
CLK
D4
D5
D6
D7

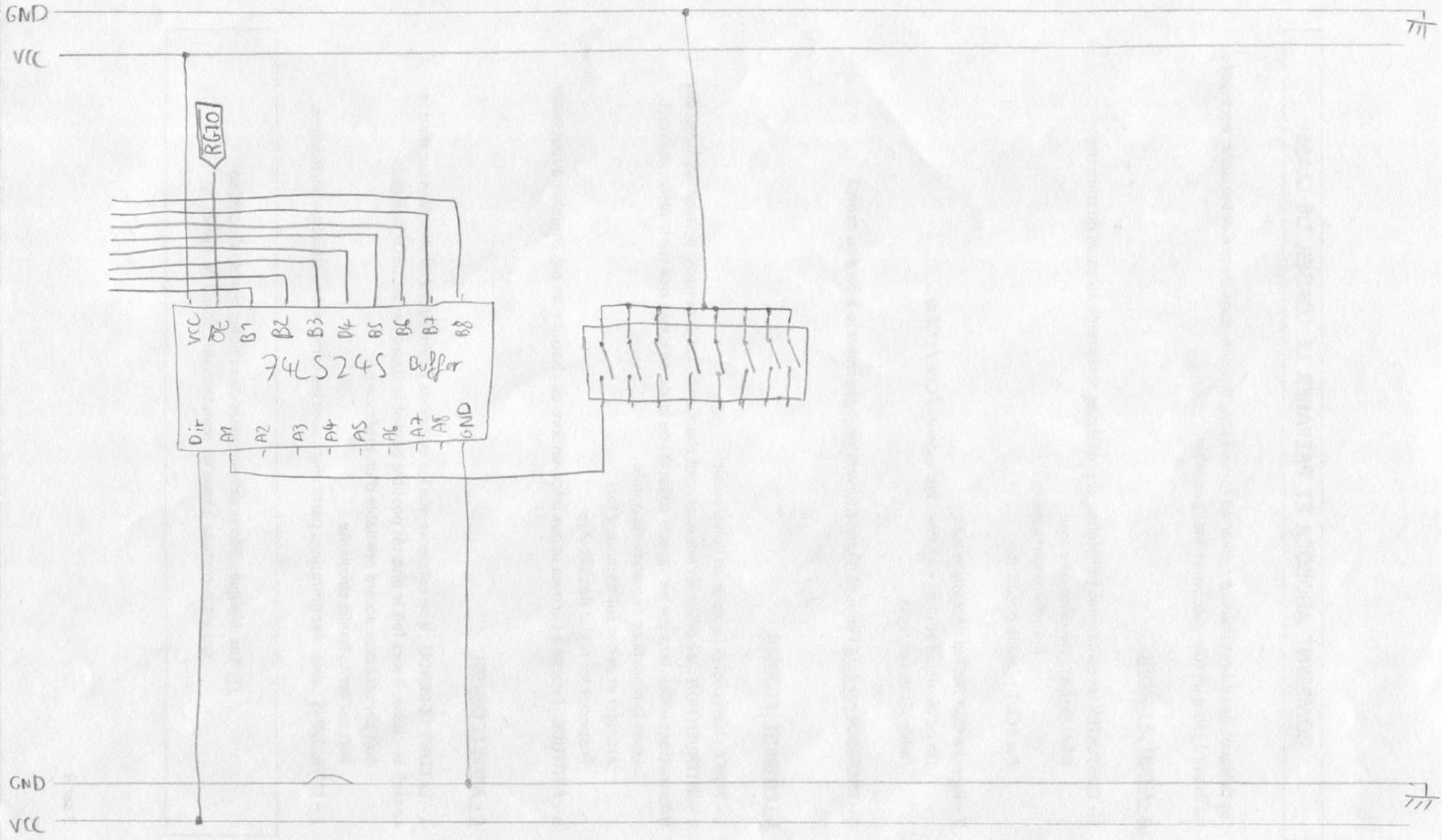

Registers
GND
VCC
74LS245
74LS273
74LS273
74LS08
DIR
GND
VCC
RGA2
RGB2
CLK
ALUO
Flagsclk
RGO2
RGOclk

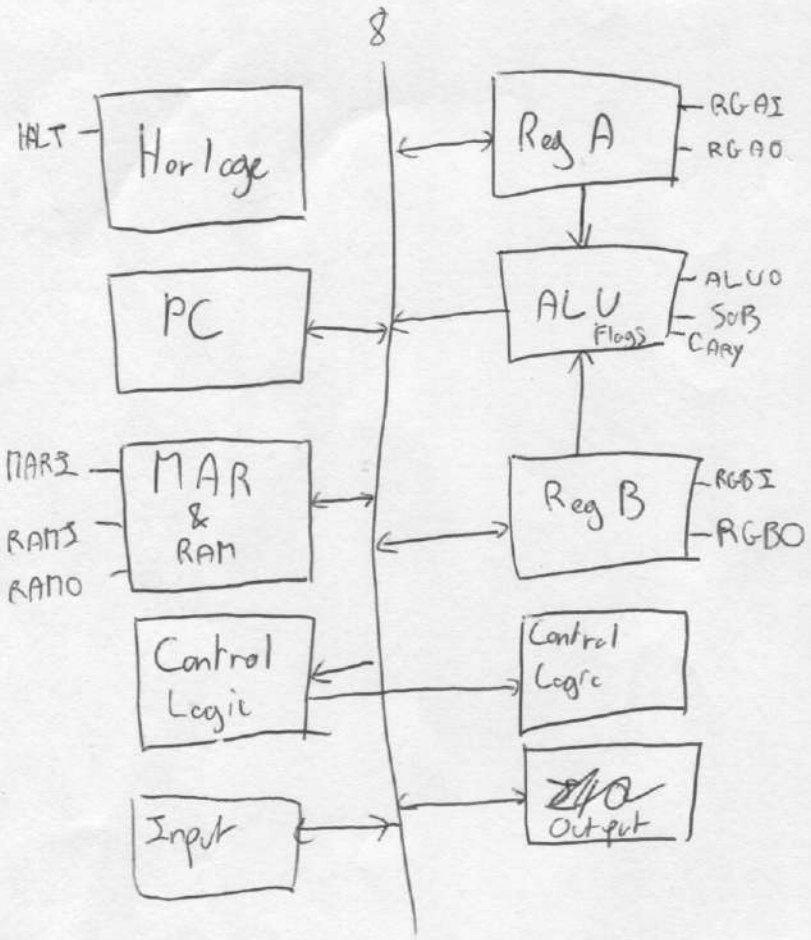

ALU
GND
Vcc
ALU0
74LS245
74LS283
74LS283
74LS86
74LS86
SUBS
GND
Vcc
PlogsUA
74LS174
74LS08
74LS02
ALU0
ALU0
74LS04
N
C
Z
GND
Vcc

Out Register



In Register


GND
VCC
RG10
VCC
OE
B1
B2
B3
B4
B5
B6
B7
B8
74LS245 Buffer
Dir
A1
A2
A3
A4
A5
A6
A7
A8
GND
GND
VCC



Jeu d'instructions

HLT
NOP
ADD
ADC
SUB
SUC
JMP
JMPC
JMPN
JMPZ
OUT
IN (?)
LDA
STA
LDB
STB
LDI

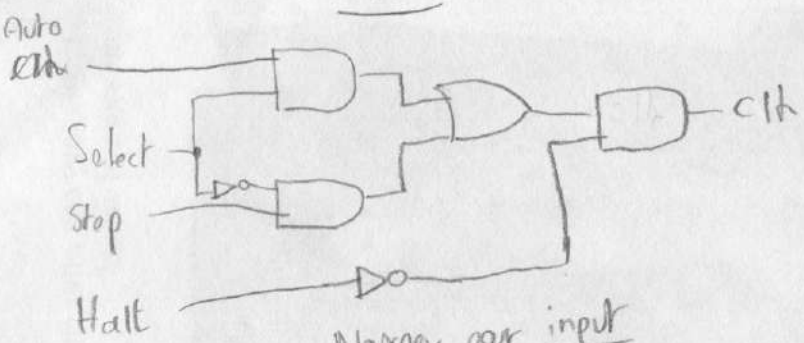
Caractéristiques

- Bus de données 8 bits
- 256o de mémoire
- Module d'entrée
- LCD?

Ben Eater

CLK	PC
MAR	A Flags
RAM	ALU
RAM	B Zero-test
IR	Out
Step	Divers
Microcode	Signaux CTRL

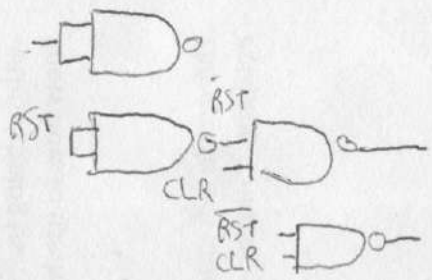
Actuel



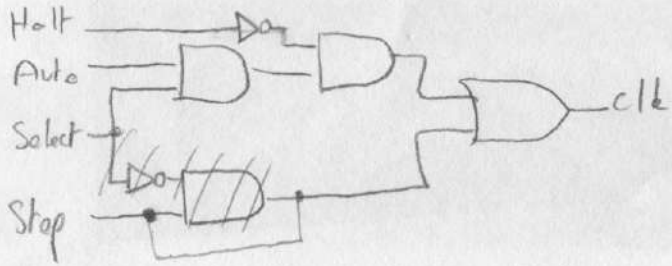
Instruction IN:

0	PGCO, MARI
1	RAMO, IRGI
2	HALT, RGAI, RGIO
3	CLR

Reset Circuit



Nouveau par input



	P	F	A	E	G	C	D
0	1	1	1	1	0	1	1
1	1	0	0	0	0	1	0
2	1	0	1	1	1	0	1
3	1	0	1	0	1	1	1
4	1	1	0	0	1	1	0
5	0	1	1	0	1	1	1
6	0	1	1	1	1	1	1
7	1	0	1	0	0	1	0
8	1	1	1	1	1	1	1
9	1	1	1	0	1	1	1

7B	
42	
5D	
57	
66	
37	
3F	
52	
7F	
77